FIELD-EFFECT TRANSISTOR MADE BY FUNCTIONALIZED PENTACENE WITH LOGIC GATE APPLICATION

J.G. Park, R. Vasic (NHMFL); J.S. Brooks (NHMFL / FSU Physics); J.E. Anthony (U. of Kentucky, Chemistry)

Introduction

By attaching a functional side group, soluble and stable functionalized pentacene, 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) can be made [1]. Transport measurements on single crystals show anisotropic conducting properties [2], and persistent photoconductivity is also present in single crystalline samples [3]. The application of the functionalized pentacene materials to field-effect transistor (FET) structures has been demonstrated [4] with room temperature mobilities up to 0.4 cm^2/Vs.

Experimental

A TIPS-pentacene was thermally evaporated at a base pressure less than 5×10^{-6} Torr. A heavily doped n-type Si substrate (ρ < 0.002 Ωcm) served as a back gate. A thermally grown 300 nm SiO_2 layer was used for the gate dielectric without molecular modification. Electrical characterization was performed using a HP 4155C semiconductor parameter analyzer.

Results and Discussion

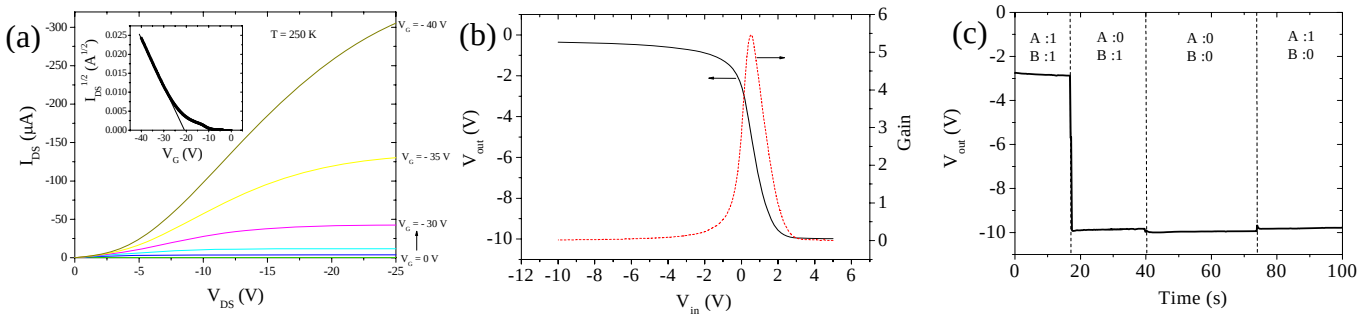

Fig. 1 (a) shows typical output characteristics for a TIPS-pentacene FET at room temperature and the inset shows the transfer characteristics in the saturation regime(V_{DS} = -25 V). We have fabricated inverter (NOT) using p-type TIPS-pentacene FET and off-chip resistor (Fig. 1 (b)). A FET with room temperature mobility of 0.002 cm^2/Vs (thickness of 50 nm) and serial resistor of 10 MΩ were combined for inverter. When the input voltage is $V_{in} \geq 2$ V (logical *0*), the transistor resistance is larger than resistor, therefore V_{out} = -10 V (logical *1*). When V_{in} = - 10 V (logical *1*), the transistor resistance is lower than series resistor and V_{out} = 0 V (logical *0*). The maximum gain defined by dV_{out}/dV_{in} is up to 5.5. With an additional FET in series, NAND (Fig. 1 (c)) logic gates can be constructed.

Acknowledgements

This work is supported by NSF-DMR-0203532 (JSB) and Office of Naval Research (JEA). JGP thanks MARTECH for access to processing facilities.

References

[1] Anthony, J.E., *et al.*, Org. Lett., **4**, 15 (2002).
[2] Brooks, J.S., *et al.*, Curr. Appl. Phys., **1**, 301 (2001).
[3] Brooks, J.S., *et al.*, J. Appl. Phys., **96**, 3312 (2004).
[4] Sheraw, C.D., *et al.*, Adv. Mater., **15**, 2009 (2003).